Claims

What is claimed is:

1. A method for providing verification for a first simulation image, comprising:
   removing nodes from the first simulation image to produce an optimized image and an optimized nodes image;
   simulating the optimized image;
   invoking the optimized nodes image if debugging is selected;
   reconstructing a second simulation image using the optimized image and the optimized nodes image;
   simulating the second simulation image to gather simulation data; and
   debugging the first simulation image using simulation data.

2. The method of claim 1, wherein the first simulation image and the second simulation image comprise a register transfer level design.

3. The method of claim 2, wherein debugging comprises comparing a reference value to a value of a corresponding register transfer level design component of at least one selected from the group consisting of the optimized image and the second simulation image.

4. The method of claim 1, wherein the optimized nodes image comprises at least one node selected from the group consisting of a redundant node, an unobservable node, and a dangling node.

5. The method of claim 1, wherein the optimized nodes image comprises a list of optimized nodes and information about how to compute the optimized nodes image from the optimized image.

6. The method of claim 1, wherein simulating is performed on a simulation test bench.

7. The method of claim 1, further comprising:

isolating and eliminating a bug in the first simulation image using simulation data.

8. A computer system for providing verification for a simulation image, comprising:

a processor;

a memory;

a storage device; and

software instructions stored in the memory for enabling the computer system to:

remove nodes from the first simulation image to produce an optimized image and an optimized nodes image;

simulate the optimized image;

invoke the optimized nodes image if debugging is selected;

reconstruct a second simulation image using the optimized image and the optimized nodes image;

simulate the second simulation image to gather simulation data; and

debug the first simulation image using simulation data.

9. The computer system of claim 8, wherein the first simulation image and the second simulation image comprise a register transfer level design.

10. The computer system of claim 9, wherein debugging comprises comparing a reference value to a value of a corresponding register transfer level design component of at least one selected from the group consisting of the optimized image and the second simulation image.

11. The computer system of claim 8, wherein the optimized nodes image comprises at least one node selected from the group consisting of a redundant node, an unobservable node, and a dangling node.

12. The computer system of claim 8, wherein the optimized nodes image comprises a list of optimized nodes and information about how to compute the optimized nodes image from the optimized image.

13. The method of claim 8, wherein simulating is performed on a simulation test bench.

14. The computer system of claim 8, further comprising a software instruction to:
isolate and eliminate a bug in the second simulation image using simulation data.

15. A system for verifying a first simulation image, comprising:
an optimizer tool providing functionality to optimize the second simulation image into an optimized image and an optimized nodes image;
a test vector providing an input signal value for a component in at least one selected from the group consisting of the optimized image and a second simulation image; and
a reconstructor tool of a testbench providing functionality to reconstruct the second simulation image using the optimized image and the optimized nodes image, if debugging is selected,
wherein the testbench provides functionality to verify at least one selected from the group consisting of the optimized image and the second simulation image using the test vector.

16. The system of claim 15, wherein the first simulation image and the second simulation image comprise a register transfer level design.

17. The system of claim 16, wherein debugging comprises comparing a reference value to a value of a corresponding register transfer level design component of at least one selected from the group consisting of the optimized image and the second simulation image.

18. The system of claim 15, wherein the optimized nodes image comprises at least one node selected from the group consisting of a redundant node, an unobservable node, and a dangling node.

19. The system of claim 15, wherein the optimized nodes image comprises a list of optimized nodes and information about how to compute the optimized nodes image from the optimized image.

20. An apparatus providing verification for a first simulation image, comprising:

means for removing nodes from the first simulation image to produce an optimized image and an optimized nodes image;

means for simulating the optimized image;

means for invoking the optimized nodes image if debugging is selected;

means for reconstructing a second simulation image using the optimized image and the optimized nodes image;

means for simulating the second simulation image to gather simulation data; and

means for debugging the first simulation image using simulation data.